Product Bulletin

Texas Instruments Gen 2 Integrated Circuit:

Gen 2 IC Based on EPCglobal Gen 2 Specification

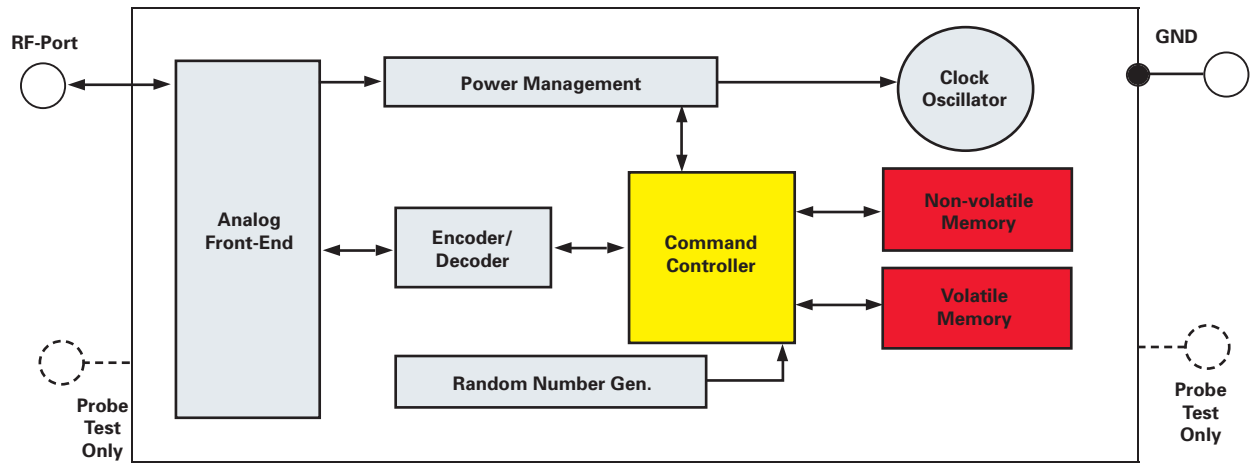
Key Features

- Meets EPCglobal Gen 2 (v. 1.0.9) and ISO/IEC 18000-6c
- Global frequency operability, 860-960 MHz
- Supports optional Gen 2 commands: Block Write and Block Erase
- 192-bit memory: 96-bit EPC, 32-bit access password, 32-bit kill password, 32-bit TID memory (factory programmed and locked)
- Designed for high-performance, low power consumption based on the most advanced silicon process node for RFID (130 nm)
- Fast tag singulation using the most advanced anti-collision scheme
- Suitable for E-field and H-field applications
- RoHS compliant

Since 1989, Texas Instruments has been manufacturing ICs for a wide array of RFID applications. This heritage has provided TI with strong expertise in the design of ICs used in RFID, and the high quality manufacturing and testing techniques developed over the years have separated TI from the competition. Being a global leader in integrated circuit design and fabrication allows TI to leverage its core strengths and deliver a UHF Gen 2 chip built on the company's 130 nm process node.

The Gen 2 chip is intended for use in the manufacture of passive RFID tag products operating in the 860 to 960 MHz frequency band. Meeting all of the EPCglobal Gen 2 and ISO/IEC 18000-6c required specifications with 192 bits of memory, this chip also goes beyond the standard requirements to provide additional functionality by supporting "block write" and "block erase" commands. This important feature provides faster data communication between the tag and the reader/interrogator. In addition, the chip incorporates a Shottky diode that provides increased tag sensitivity, allowing for longer read range and a more reliable read/write exchange between the tag and the reader. The Shottky diode also allows for faster tag singulation, plus the chip incorporates the Gen 2 protocol anti-collision scheme to further improve read accuracy.

While primarily intended for the supply chain market, the Gen 2 chip may also be used in asset tracking, baggage tagging, manufacturing, and a wide assortment of other applications where long read range is required. The chip is available in raw wafer form, or bumped, back ground, and sawed. A wafer map is also provided.



Simplified block diagram.

Specification Table

Protocol	EPCglobal Gen 2 specification (V 1.0.9)
Frequency	860 – 960 MHz
Communication Mode	Half Duplex, Reader talks first
Data rate	Uplink: 40 to 640 Kbps, Downlink: 40 to 160 Kbps
Modulation	Downlink: ASK or PR-ASK, Uplink: ASK
Operating Temperature	–40°C to + 65°C
Chip Size	0.7 x 0.8 mm x 0.015 mm
Commands Supported	EPCglobal Class 1 Gen 2 and ISO/IEC 18000-6c mandatory commands, optional block write and erase
Encoding	Uplink: FM0, Miller, Downlink: PIE
Read Range	7.0 m, (6.6 m in Europe) typical*

** Read range distance is for reference only. Actual read range distance may vary according to tagged materials, antenna design, reader, and environmental circumstances. Maximum tag write distance is 70% of read distance.*

Wafer Ordering Information

Part Number	Bumped	Backgrind	Sawn	Wafer Map	Wafer size
RX-UHF-11111-01	Yes	Yes	Yes	Yes	8" (200 mm)
RX-UHF-00001-01	No	No	No	Yes	8" (200 mm)

For more detailed information, please visit the document center at www.ti.com/rfid. The EPC Gen 2 integrated circuit is also available in a "Strap" form factor (part # RI-UHF-STRAP-02).

Additional information on the strap version and all of the RFID products from Texas Instruments is available on our web site.

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